Announcements

- Exam #2 regrade requests due today.
- Homework #8 due today.
- Final Exam: Th June 12, 8:30-10:20am, CMU 120 (extension to 11:20am requested).
- Grades available for viewing via Catalyst.

CMOS Inverter
Performance Scaling

- State-of-the-art short gate length technologies are hard to analyze
- Scaling can be used to properly set W/L for a given load capacitance relative to reference gate simulation with a reference load.

$$\tau_P = \frac{(W/L)}{(W/L)'} \times \left(\frac{C_L'}{C_{Lref}} \right) \times \tau_{Pref} \quad \text{or} \quad \left(\frac{W}{L} \right)' = \left(\frac{W}{L} \right) \times \left(\frac{\tau_{Pref}}{\tau_P} \right) \times \left(\frac{C_L'}{C_{Lref}} \right)$$

Scaling allows us to calculate a new geometry (W/L)' in terms of a target load and delay.

CMOS Inverter

Performance Scaling

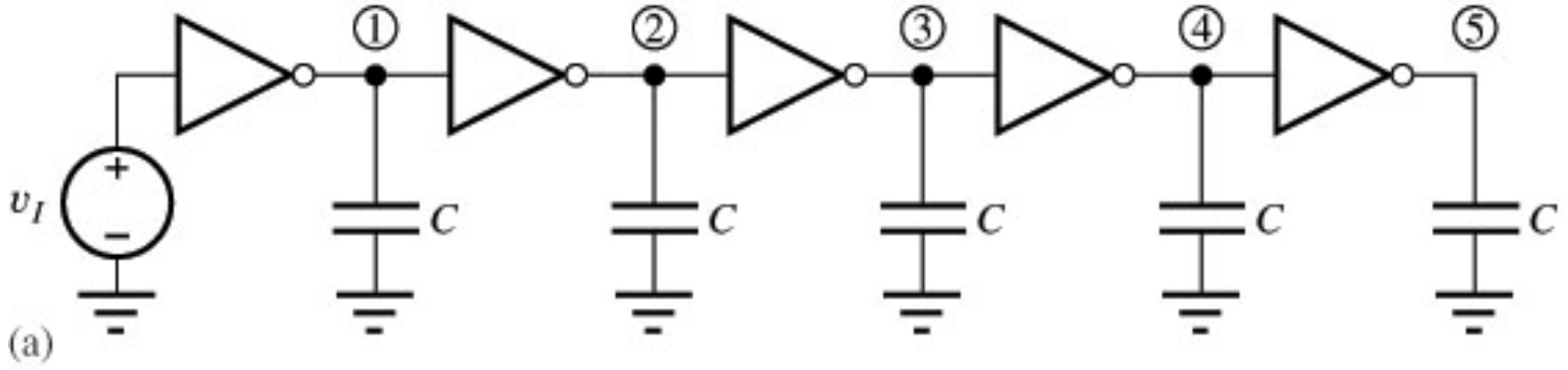
- Consider a reference inverter with a delay of 3.16 ns.
- What is the delay if an inverter has a W/L 4x larger than the transistors of the reference inverter and twice the load capacitance.

$$\tau_P = \frac{(2/1)}{(8/1)'} \times \left(\frac{2pF'}{1pF} \right) \times \ 3.16 \ \ ns = 1.58 \ \ ns$$

Scaling allows us to calculate a new geometry (W/L)' or delay relative to a reference design.

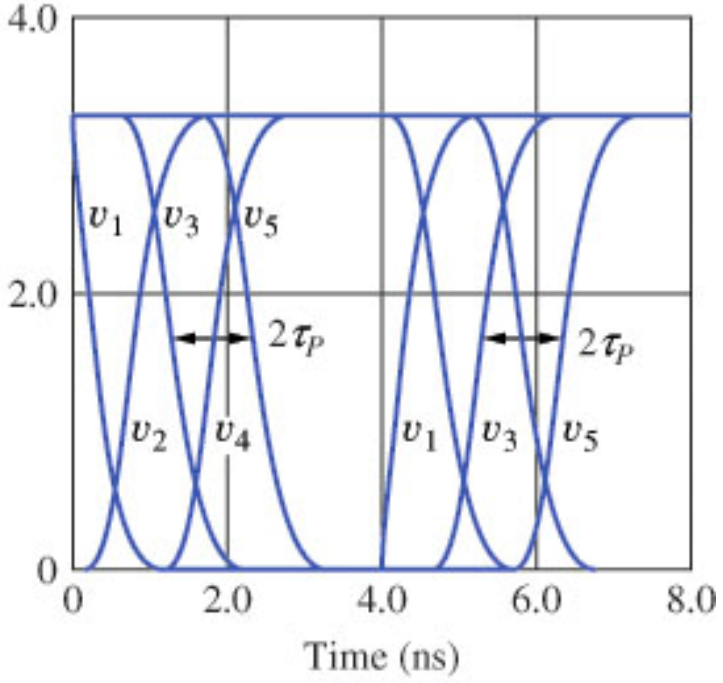
CMOS Logic
Delay of Cascaded Inverters

- An ideal step was used to derive the previous delay equations, but this is not possible to implement
- By using putting the following circuit in SPICE, it is possible to produce more accurate



CMOS Logic
Delay of Cascaded Inverters (cont.)

- The simulated output of the previous circuit appears below, and it can be seen that the delay for the nonideal step input is approximately twice than the ideal case:



$$\tau_{PHL} \cong 2.4 R_{onN} C$$

$$\tau_{PLH} \cong 2.4 R_{onP} C$$

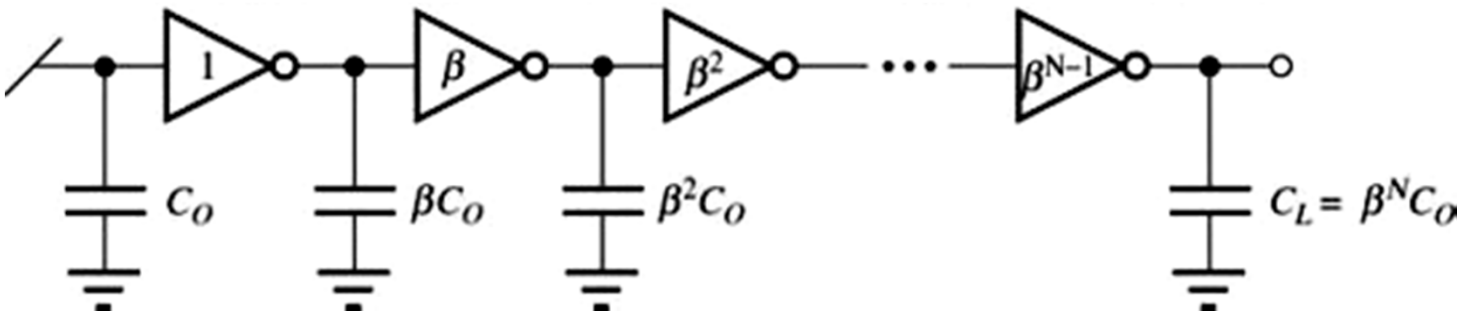
$$t_f = 2\tau_{PHL}$$

$$t_r = 2\tau_{PLH}$$

Cascade Buffers

Driving Large Capacitances

- In some circuits, the logic must be able to drive large capacitances (10 to 50 pF)
- By cascading a number of increasingly larger inverters, it is possible to drive the loads



Cascade Buffers

Inverter Sizing

- The taper factor β determines the increase of the cascaded inverter's size in manner shown of the previous image.

$$\beta^N = \frac{C_L}{C_o}$$

where C_o is the unit inverter's load capacitance

- The delay of the cascaded buffer is given by the following:

$$\tau_B = N\left(\frac{C_L}{C_o}\right)^{1/N} \tau_o$$

where τ_o is the unit inverter's propagation delay

Cascade Buffers

Optimum Design

- The following expressions can aid in the design of an optimum cascaded buffer

$$N_{opt} = \ln\left(\frac{C_L}{C_o}\right)$$

$$\beta_{opt} = \left(\frac{C_L}{C_o}\right)^{\frac{1}{\ln\left(\frac{C_L}{C_o}\right)}} = \varepsilon$$

$$\tau_{Bopt} = \ln\left(\frac{C_L}{C_o}\right)\varepsilon\tau_o$$

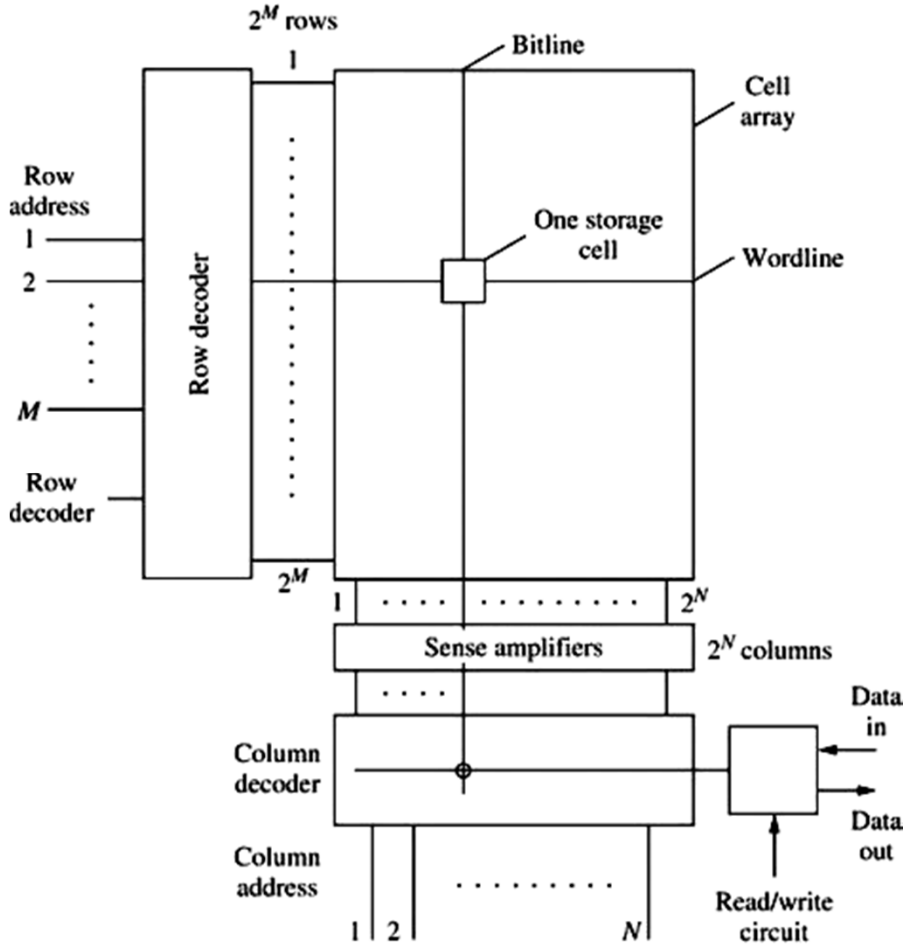
EE 331 Devices and Circuits I

Chapter 8
MOS Memory

Random Access Memory

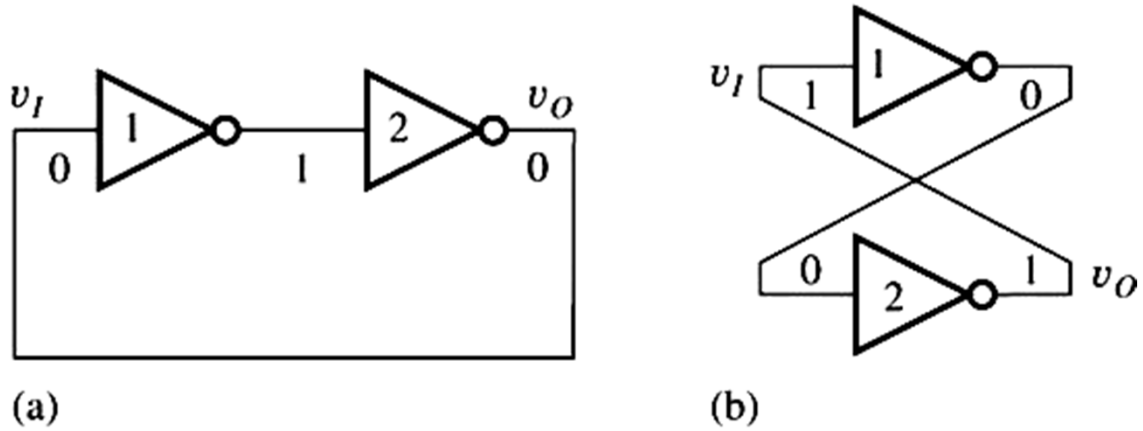
- Random Access Memory (RAM) refers to memory in a digital system that has both read and write capabilities and any location is directly accessible
- Static RAM (SRAM) is able to store its information as long as power is applied, and it does not lose the data during a read cycle
- Dynamic RAM (DRAM) uses a capacitor to temporarily store data which must be refreshed periodically to prevent information loss, and the data is lost in most DRAMs during the read cycle
- SRAM takes approximately four times the silicon area of DRAM

A 256-Mbit Memory Chip



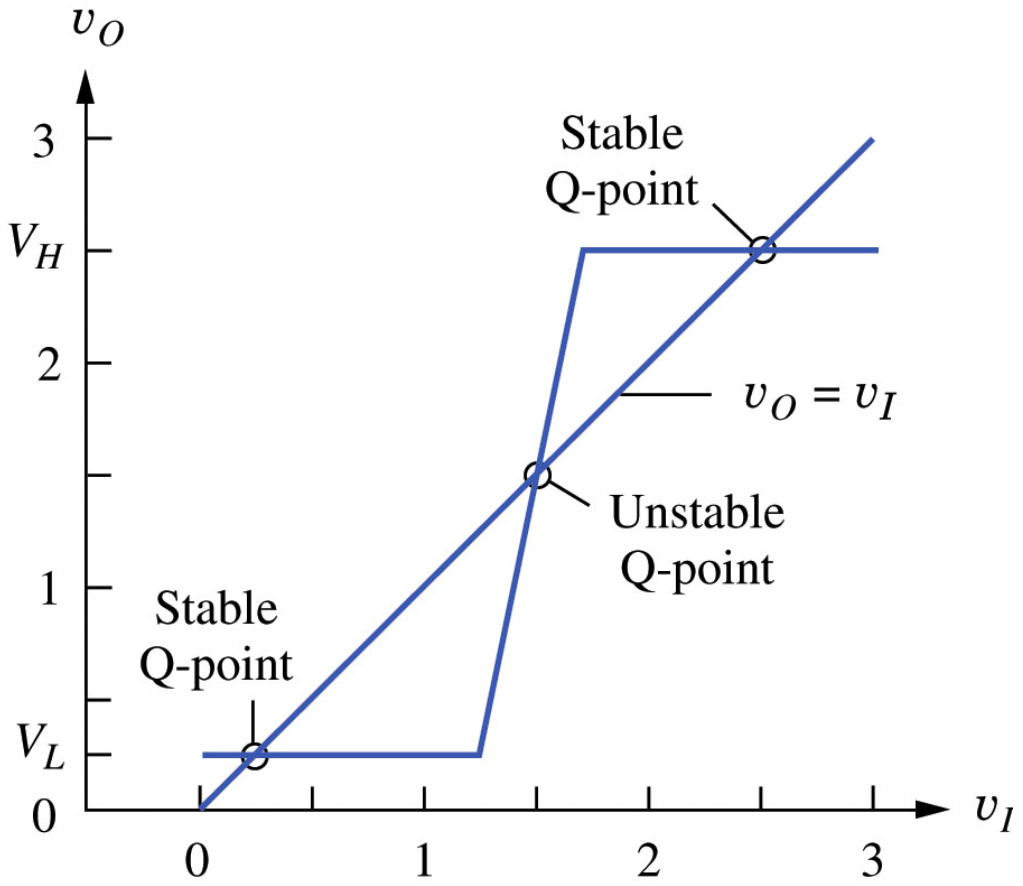
- The memory block diagram contains 2^{M+N} storage locations (M columns x N rows)
- When a bit is selected, the set of sense amplifiers are used to read/write to the memory location
- Horizontal rows are referred to as wordlines, whereas the vertical lines are called bitlines

Static Memory Cells



- Inverters configured as shown in the above figure form the basic static storage building block (note the schematics represent two drawings of the same circuit)
- These cross-coupled inverters are often referred to as a latch
- The circuit uses positive feedback

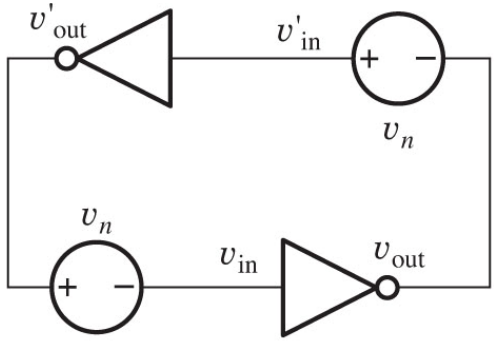
Static Memory Cells VTC

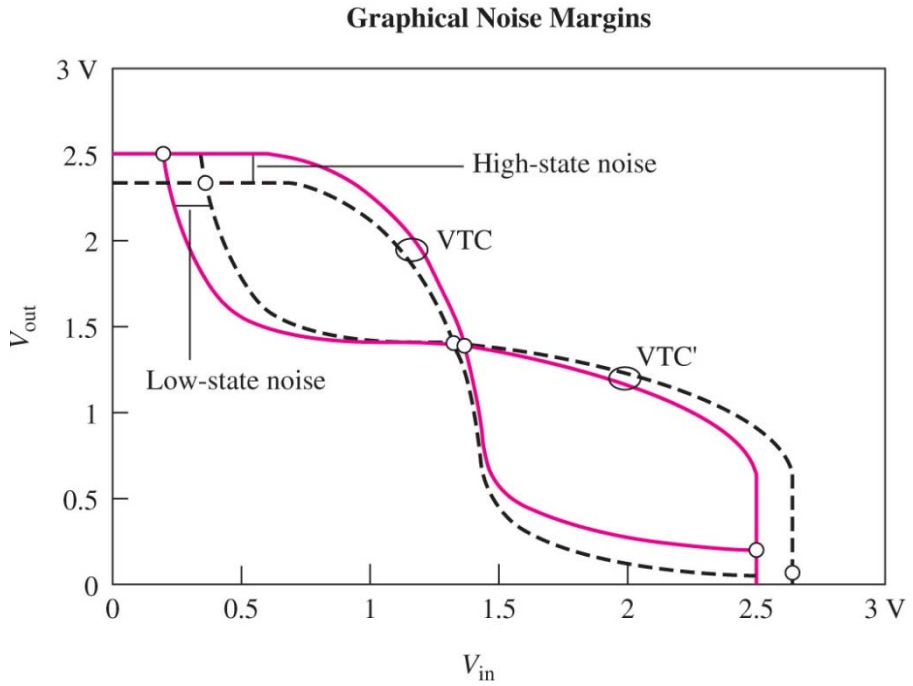


- The previous latch has only two stable states and is termed bistable
- However, it is possible for the circuit to be held at an unstable equilibrium point where slight changes in the voltage will cause it to latch in one of the stable states

Static Noise Margins

Graphical Approach

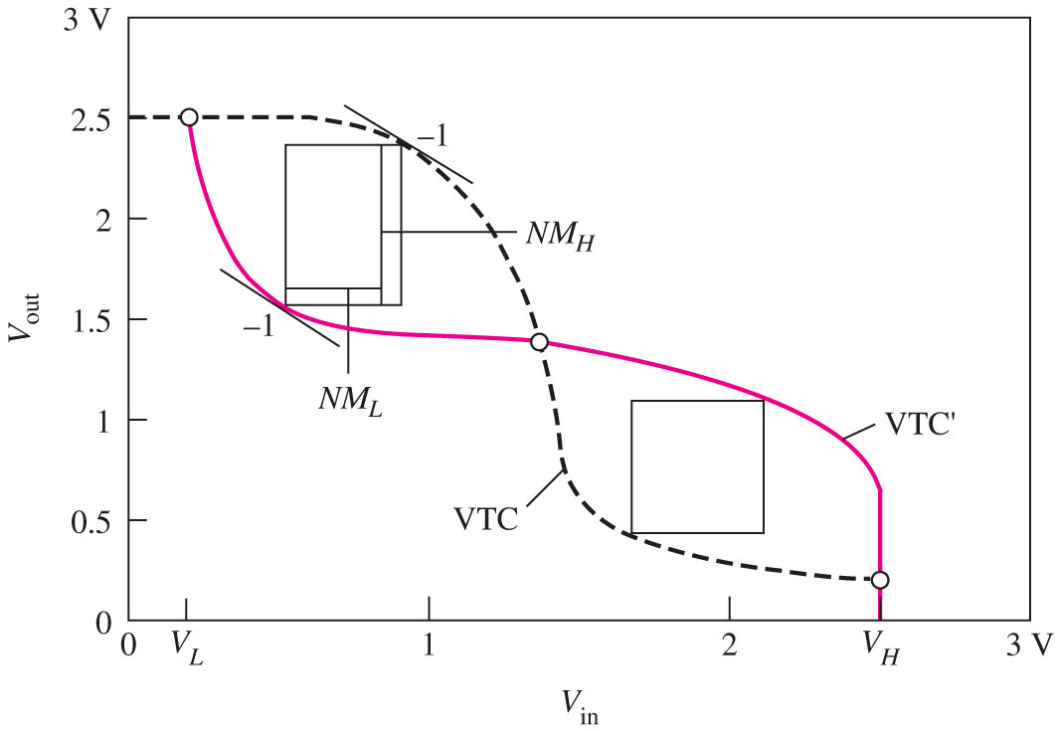




"Butterfly" diagram is produced by plotting v_{out} vs. v_{in} and v'_{in} vs. v'_O for the inverters.
Noise shifts the characteristics.

Static Noise Margins

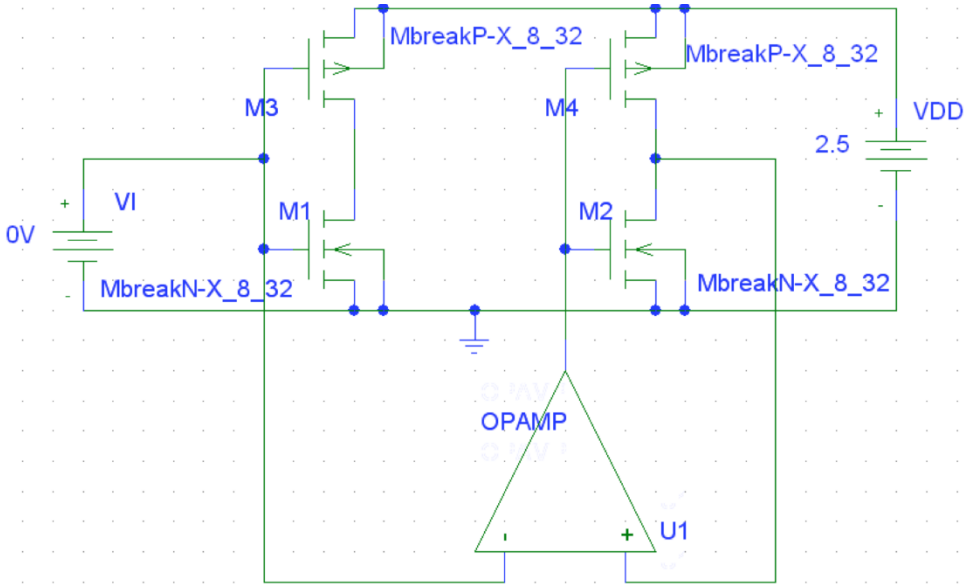
Graphical Approach

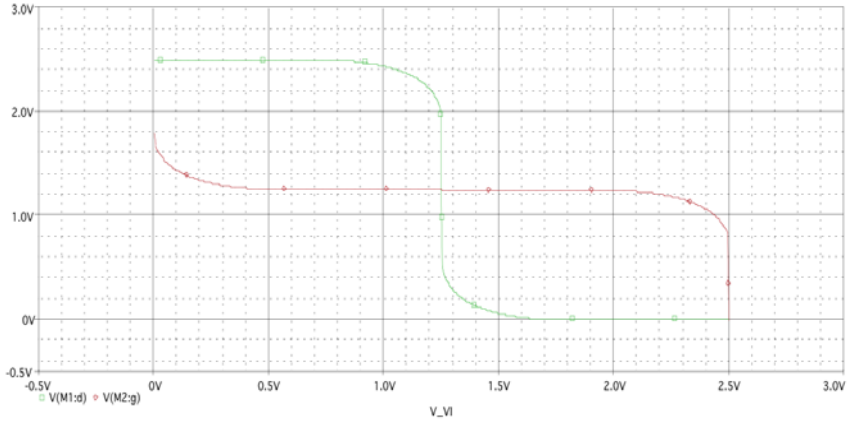


- "Butterfly" diagram is produced by plotting v_{out} vs. v_{in} and v_{in} vs. v_o for a single inverter.
- Noise margins are defined by either the largest square or largest rectangle that can be placed between the two curves.

Static Noise Margin

Spice Simulation Circuit



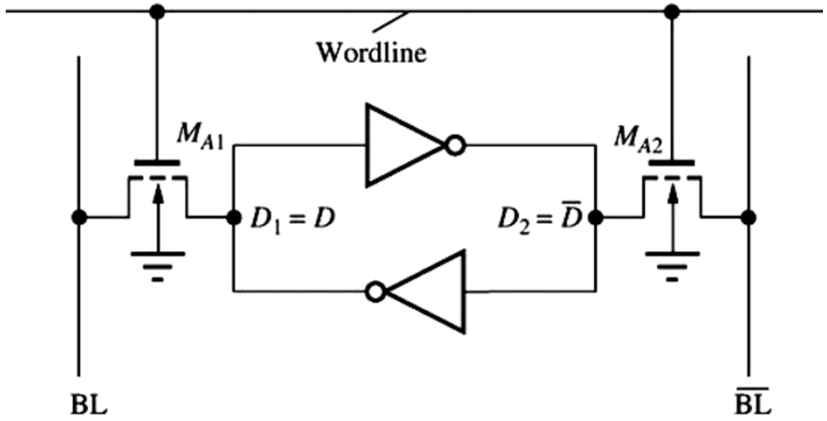


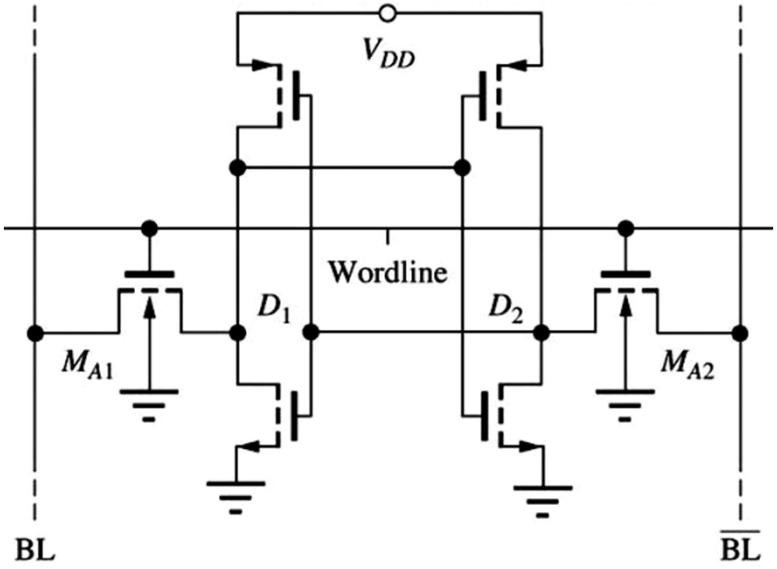
The opamp forces the output of the second inverter to equal the input of the first inverter.

The 6-T Cell

Basic Circuitry

- With the addition of two control transistors, the 6-T cell is created that stores both the true and complemented values of the data

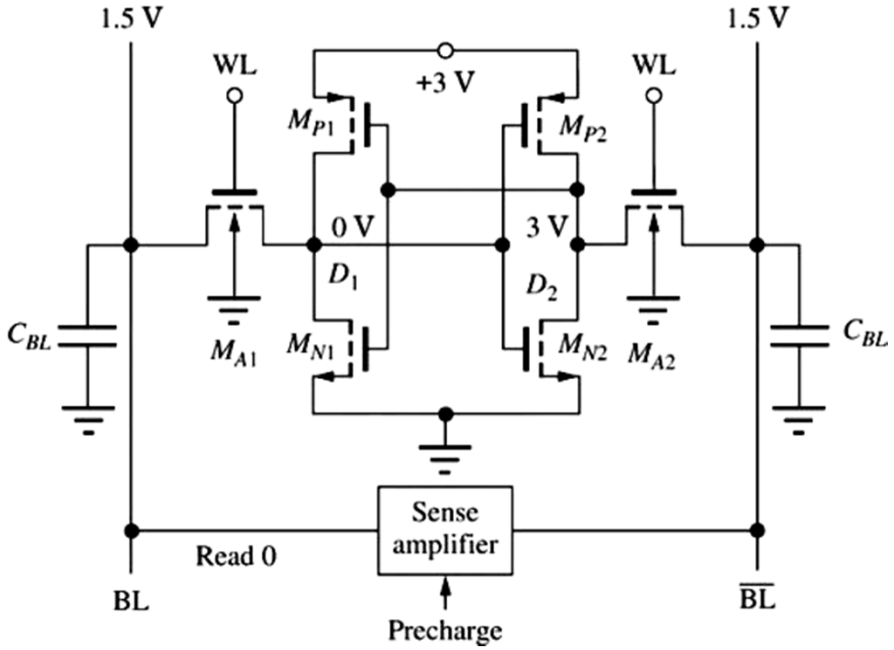




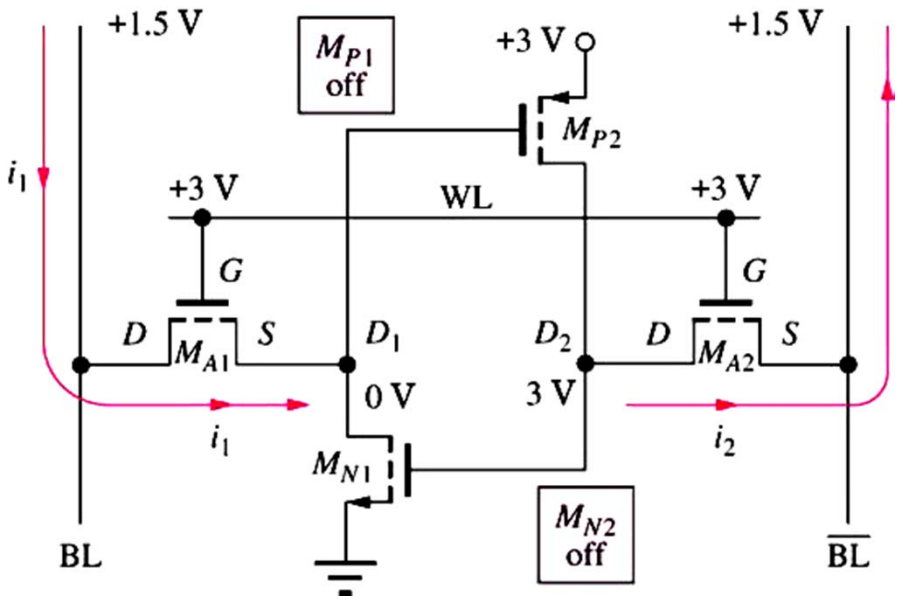
The 6-T Cell

Read Operation

Initial state of the 6-T cell storing a "0" with the bitlines' initial conditions assumed to $V_{DD}/2$



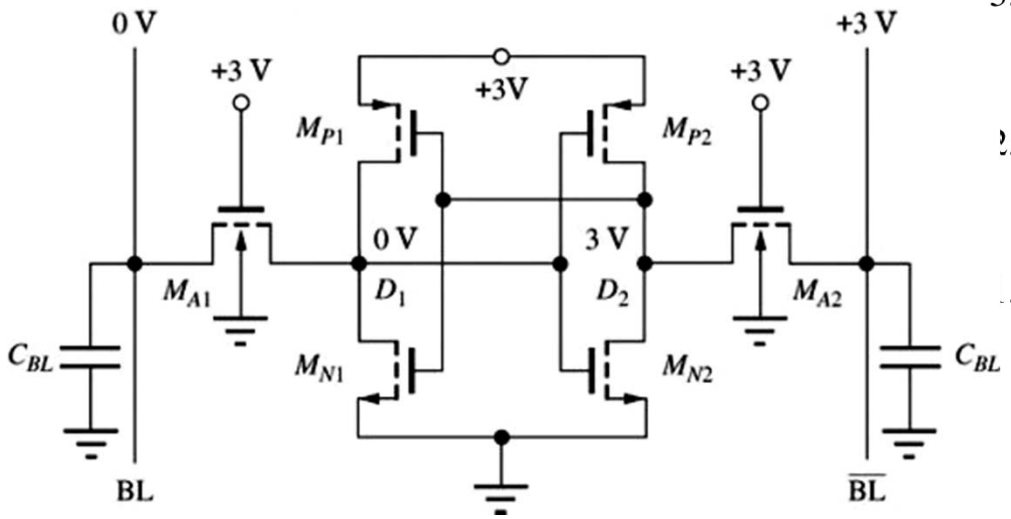
Conditions immediately after the WL transistors have been turned on



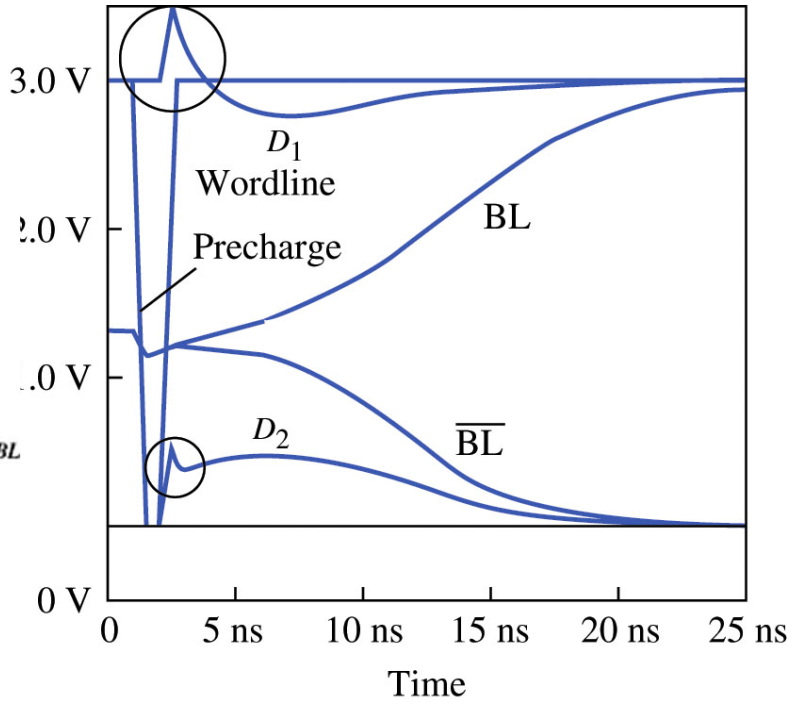
The 6-T Cell

Read Operation (cont.)

Final read state for the 6-T cell



Waveforms of the 6-T cell read operation



The 6-T Cell

Read Operation (cont.)

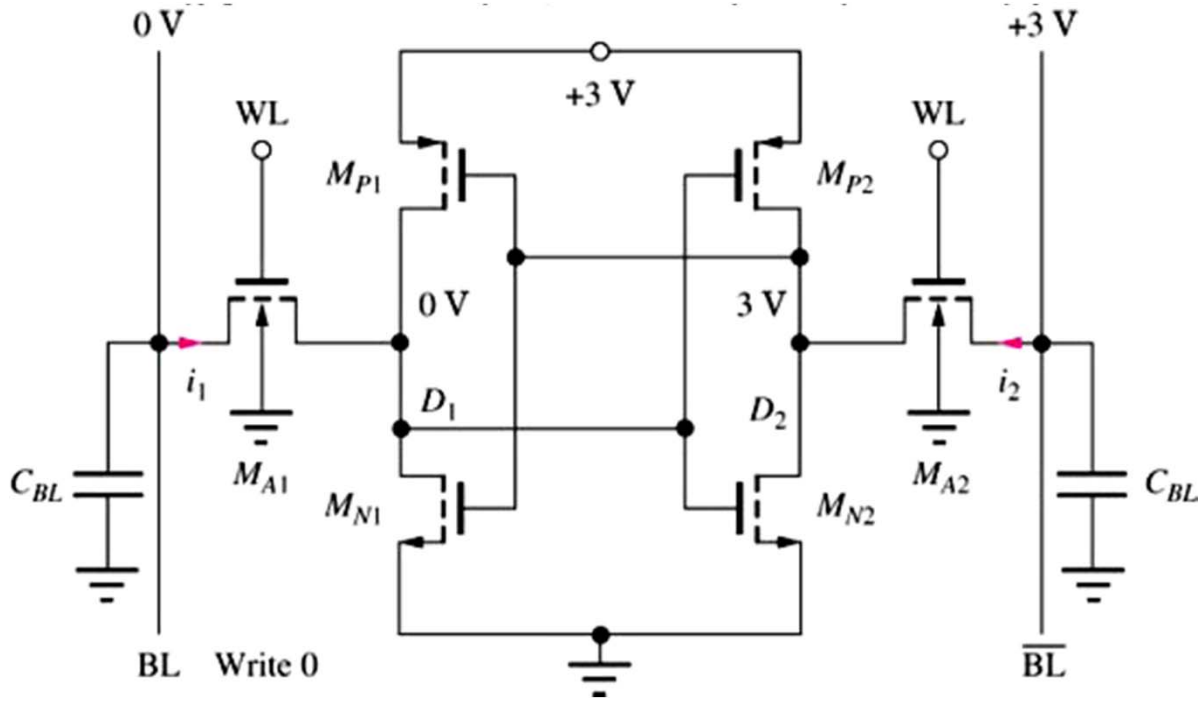
- Reading a 6-T cell that is storing a "1" follows the same concept as before, except that the sources and drains of the WL transistors are switched

- Note that the delay is approximately 20ns for this particular cell

The 6-T Cell

Write Operation

It can be seen that not much happens while writing a “0” into a cell that already stores a “0”



The 6-T Cell

Write Operation (cont.)

While writing a "0" to a cell that is storing a "1", the bitlines must be able to overpower the output drive of the latch inverters to force it to store the new condition